Sub 100 nm: Critical Dimensions (Logic)

Node	90 nm	65 nm	45 nm	32 nm	22 nm
Lithography	248 nm dry	193 nm dry	193 nm dry	193 nm immersion + double patterning	193 nm immersion + double patterning
Process	SiGe is used to strain a silicon channel; tensile nitride layer for NMOS channel; Ni-Si replaces Co-Si	SiGe for PMOS; Poly gates; W contact, M1 in Cu	SiGe for PMOS; Metal gates with High-K; W contact; M1 in Cu	SiGe_PMOS; eSi_NMOS; Metal gates with high-K, M0 level in Cu; W contact; M1 in Cu	Tri-gate transistor; SiG3_PMOS; eSi_NMOS; Metal gates, M0 level in W; W contact; M1 in Cu
Minimum Contacted Gate Pitch (nm)	310	220	160	113	90
Minimum Gate Length (nm)	45	36	45	34	25
Minimum Metal 1 Pitch (nm)	220	210	150	113	90

90 nm and 45 nm have the same gate-length
65 nm and 32 nm have the same gate-length

Gate length is not an accurate parameter for defining technology node for devices below 100 nm node