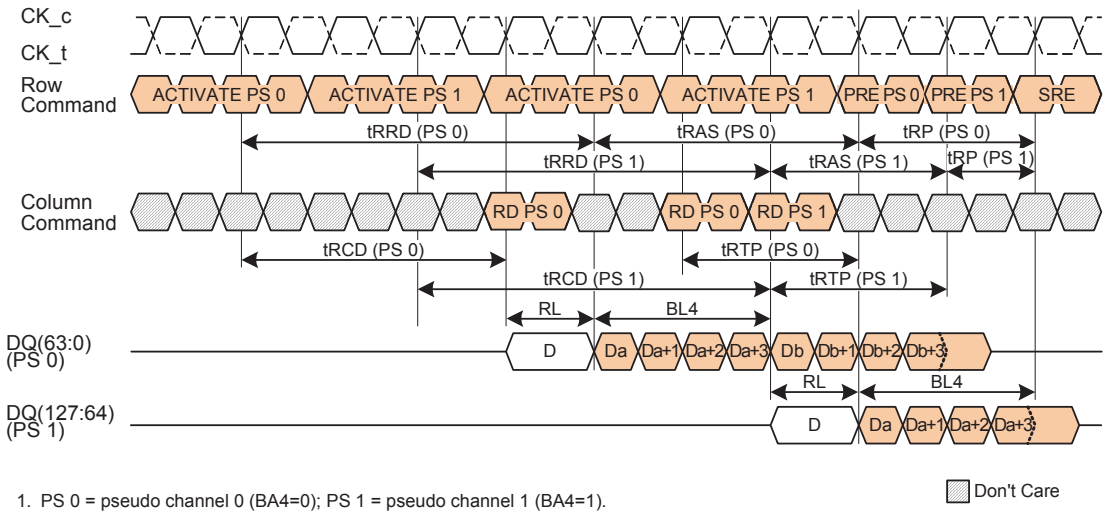
3.2.1 Legacy Mode and Pseudo Channel Mode

HBM DRAM defines two mode of operation depending on channel density. The mode support is fixed by design and is indicated on bits [17:16] of the DEVICE_ID wrapper register.

Legacy mode provides 256 bit prefetch per memory Read and Write access. Address bit BA4 is a “Don’t Care” in this mode.

Pseudo Channel mode divides a channel into two individual sub-channels of 64 bit I/O each, providing 128 bit prefetch per memory Read and Write access for each Pseudo channel. Both Pseudo channels operate semi independent: they share the channel’s row and column command bus as well as CK and CKE inputs, but decode and execute commands individually as illustrated in Figure 2. Address BA4 is used to direct commands to either to Pseudo Channel 0 (BA4 = 0) or Pseudo Channel 1 (BA4 = 1). Power-down and Self-Refresh are common to both Pseudo channels due to shared CKE pin. Array timings are calculated individually for each Pseudo channel. For commands that are common to both Pseudo channels (PDE, PDX, SRE, SRX and MRS) it is required that the respective timing conditions are met by both Pseudo channels when issuing that command. Pseudo channel mode requires that burst length is set to 4. Both Pseudo channels also share the channel’s mode registers. All I/O signals of DWORD0 and DWORD1 are associated with Pseudo channel 0, and all I/O signals of DWORD2 and DWORD3 with Pseudo channel 1.



1. PS 0 = pseudo channel 0 (BA4=0); PS 1 = pseudo channel 1 (BA4=1).
2. RL = 1 is shown as an example. Other timings parameters (tMRD, tRRD, tRAS, tRP, tRTP) are not to scale.
3. Timing parameters like tRCD, tRRD, tRAS, tRP, tRTP apply independently for pseudo channels 0 and 1.
4. Self refresh entry (SRE) requires that tRP is satisfied in both pseudo channels.

Figure 2 — Pseudo Channel Mode Operation

3.2.2 Dual Command Interfaces

To enable higher performance, HBM DRAMs exploit the increase in available signals in order to provide semi-independent row and column command interfaces for each channel. These interfaces increase command bandwidth and performance by allowing read and write commands to be issued simultaneously with other commands like activates and precharges. See Commands.